CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A method for debugging a configuration process of a ~~programmable logic~~ device having programmable logic and a JTAG interface comprising:

providing a connection between a configuration device and an input/output pin of the device having programmable logic which is separate from the JTAG interface;

initiating the configuration process for the ~~programmable logic~~ device having programmable logic;

coupling configuration process signals to [[an]] the input/output pin of the ~~programmable logic~~ device having programmable logic;

using boundary scan registers of the ~~programmable logic~~ device having programmable logic to capture the configuration process signals received at the input/output pin of the ~~programmable logic~~ device during the configuration process;

using the boundary scan registers to transfer the captured configuration process signals to a configuration analyzer during the configuration process;

analyzing the transferred configuration process signals using the configuration analyzer; and

verifying [[a]] the connection [[to]] between the configuration device and the input/output pin of the ~~programmable logic~~ device having programmable logic coupled to receive the configuration process signals.

2. (Currently Amended) The method of claim 1 further comprising programming [[a]] the configuration device coupled to the ~~programmable logic~~ device having programmable logic with a configuration bitstream.

3. (Currently Amended) The method of claim 2 wherein initiating the configuration process comprises causing the ~~programmable logic~~ device having programmable logic to send normal configuration process signals to the configuration device, thereby causing the configuration device to provide the configuration bitstream.

4. (Currently Amended) The method of claim 1 wherein initiating the configuration process comprises accessing the ~~programmable logic~~ device having programmable logic through [[a]] the JTAG interface.

5. (Currently Amended) The method of claim 4 further comprising:

executing a SAMPLE/PRELOAD instruction on the ~~programmable logic~~ device having programmable logic; and

executing an EXTEST instruction on the ~~programmable logic~~ device having programmable logic.

6. (Currently Amended) The method of claim 5 further comprising executing a BYPASS instruction on a configuration device coupled to the ~~programmable logic~~ device having programmable logic.

7. (Original) The method of claim 1 wherein analyzing the transferred configuration process signals comprises comparing the transferred configuration process signals with expected configuration process signals.

8. (Original) The method of claim 7 wherein if the transferred configuration process signals and the expected configuration process signals do not match, then correcting the configuration process.

9. (Currently Amended) A system comprising:

a ~~programmable logic~~ device having programmable logic and a JTAG interface coupled to boundary scan registers, the device coupled to receive a configuration bitstream by way of an input/output (I/O) pin separate from the JTAG interface;

a configuration device coupled to the ~~programmable logic~~ I/O pin of the device having programmable logic for providing the configuration bitstream to the ~~programmable logic~~ device having programmable logic by way of the I/O pin; and

a configuration analyzer coupled to the configuration device for driving configuration process signals through the configuration device in single steps, and coupled to the ~~programmable logic~~ device having programmable logic for controlling I/O pins of the ~~programmable logic~~ device having programmable logic and analyzing configuration process signals stored in the boundary scan registers of the ~~programmable logic~~ device having programmable logic during the configuration process;

wherein the ~~programmable logic~~ device having programmable logic, the configuration device, and the analyzer form at least part of a JTAG chain enabling verifying a connection to the input/output pin of the ~~programmable logic~~ device having programmable logic coupled to receive the configuration bitstream.

10. (Original) The system of claim 9 wherein the configuration device is a nonvolatile memory.

11. (Currently Amended) The system of claim 9 wherein the ~~programmable logic~~ device having programmable logic is a field programmable gate array.

12. (Canceled).

13. (Canceled).

14. (Original) The system of claim 9 wherein the analyzer comprises a computer running a program for analyzing the configuration data.

15. (Original) The system of claim 14 wherein the analyzer comprises a database of known configuration problems.

16. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections for debugging a configuration process of a ~~programmable logic~~ device having programmable logic and a JTAG interface, the code sections executable by a machine for causing the machine to perform the steps of:

initiating the configuration process for the ~~programmable logic~~ device having programmable logic;

coupling configuration process signals to an input/output pin of the ~~programmable logic~~ device having programmable logic, wherein the input/output pin is separate from the JTAG interface;

using boundary scan registers of the ~~programmable logic~~ device having programmable logic to capture the configuration process signals received at the input/output pin of the ~~programmable logic~~ device having programmable logic during the configuration process;

using the boundary scan registers to transfer the captured configuration process signals to a configuration analyzer during the configuration process;

analyzing the transferred configuration process signals using the configuration analyzer; and

verifying a connection to the input/output pin of the ~~programmable logic~~ device having programmable logic coupled to receive the configuration process signals.

17. (Currently Amended) A configuration analyzer for debugging a configuration process of a ~~programmable logic~~ device having programmable logic and a JTAG interface comprising:

means for receiving configuration process signals by way of an input/output pin of the ~~programmable logic~~ device having programmable logic separate from the JTAG interface;

means for stepping through the configuration process;

means for capturing configuration process signals received at the input/output pin in boundary scan registers as the configuration process signals are received by the ~~programmable logic~~ device having programmable logic at each step;

means for comparing the captured configuration process signals output by the boundary scan registers in a JTAG chain with expected configuration process signals during the configuration process; and

means for verifying a connection to the input/output pin of the ~~programmable logic~~ device having programmable logic coupled to receive the configuration process signals.